**AMENDMENTS TO THE CLAIMS:**

1. (Currently amended) A test circuit for a logical integrated circuit having an input terminal, a functional output terminal, and a scan output terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~

a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip-flops, and

means forming a scan path serially connecting said plurality of flip-flops through the respective logic gates, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, wherein:

the test pattern ~~measures~~ is used to measure an alternating current characteristic of the input terminal ~~or the functional output terminal~~ of said logical integrated circuit, and

said scan path connects the output terminal of the flip-flop located at an end of the first stage with the scan output terminal of said logical integrated circuit.

2. (Currently amended) A test circuit for a logical integrated circuit having a functional input terminal, an output terminal, and a scan input terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops ~~connected in series,~~

a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip-flops, and

means forming a scan path serially connecting said plurality of flip-flops through the respective logic gates, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, wherein:

the test pattern ~~measures~~ is used to measure an alternating current characteristic of ~~the functional input terminal or~~ the output terminal of said logical integrated circuit, and

said scan path connects the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage.

3. (Currently amended) A test circuit for a logical integrated circuit having an input terminal, a functional output terminal, and a scan output terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~

a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip-flops, and

means forming a scan path serially connecting said plurality of flip-flops through the respective logic gates, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, wherein:

the test pattern ~~measures~~ is used to measure an alternating current characteristic of the input terminal ~~or the functional output terminal~~ of said logical integrated circuit,

said scan path connects the scan input with the input terminal of the flip-flop located at the head of the nth stage,

from the output terminal of the flip-flop located at the end of the nth stage, said scan path further connects the flip-flops in the second to the (n-1)th stages in series,

said scan path then connects the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage, and

the scan path finally connects the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit.

4. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

an input terminal,

a functional output terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~

a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip-flops, and

means forming a scan path serially connecting said plurality of flip-flops through the respective logic gates, to propagate a test pattern applied to the input terminal of one of said

plurality of serially connected flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of the input terminal ~~or the functional output terminal~~ of said logical integrated circuit by inspecting an output of the scan output terminal of said logical integrated circuit, said method comprising:

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the input terminal of said logical integrated circuit by inspecting the output of the scan output terminal of said logical integrated circuit.

5. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a functional input terminal,

an output terminal,

a scan input terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~

a like plurality of logic gates, each logic gate having an output terminal connected to

an input terminal of a respective one of said plurality of flip-flops, and

means forming a scan path serially connecting said plurality of flip-flops through the respective logic gates, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of ~~the functional input terminal or~~ the output terminal of said logical integrated circuit by inspecting an output of the output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the scan input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the output terminal of said logical integrated circuit by inspecting the output of the output terminal of said logical integrated circuit.

6. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a functional input terminal

a functional output terminal,

a scan input terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~

a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip-flops, and

means forming a scan path serially connecting said plurality of flip-flops through the respective logic gates, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of the functional input terminal ~~or the functional output terminal~~ of said logical integrated circuit by inspecting an output of the scan output terminal of said logical integrated circuit, said method comprising:

~~connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,~~

connecting the output terminal of the flip-flop located at the end of the nth stage with the input terminal of the flip-flop located at the head of the second stage,

connecting the flip-flops in the second to the (n-1)th stages in series,

connecting the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage,

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a scan input signal to the scan input terminal of said logical integrated

circuit,

inputting a predetermined data signal to the functional input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the functional input terminal of said logical integrated circuit by inspecting ~~an~~ the output of the scan output terminal of said logical integrated circuit.

7. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a functional input terminal

a functional output terminal,

a scan input terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~

a like plurality of logic gates, each logic gate having an output terminal connected to an input terminal of a respective one of said plurality of flip-flops, and

means forming a scan path serially connecting said plurality of flip-flops through the respective logic gates, to propagate a test pattern applied to the input terminal of one of said plurality of flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of ~~the functional input terminal or~~ the functional output terminal of said

logical integrated circuit by inspecting an output of the output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

connecting the output terminal of the flip-flop located at the end of the nth stage with the input terminal of the flip-flop located at the head of the second stage,

~~connecting the flip-flops in the second to the (n-1)th stages in series,~~

connecting the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage,

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the scan input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the functional output terminal of said logical integrated circuit by inspecting the output of the output terminal of said logical integrated circuit.

8. (Currently amended) A test circuit for a logical integrated circuit having an input terminal, a functional output terminal, and a scan output terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops,

~~connected in series,~~ and

means forming a scan path serially connecting said plurality of flip-flops, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, wherein:

the test pattern ~~measures~~ is used to measure an alternating current characteristic of the input terminal ~~or the functional output terminal~~ of said logical integrated circuit, and

said scan path connects the output terminal of the flip-flop located at an end of the first stage with the scan output terminal of said logical integrated circuit.

9. (Currently amended) A test circuit for a logical integrated circuit having a functional input terminal, an output terminal, and a scan input terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~ and

means forming a scan path serially connecting said plurality of flip-flops, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, wherein:

the test pattern ~~measures~~ is used to measure an alternating current characteristic of ~~the functional input terminal or~~ the output terminal of said logical integrated circuit, and

said scan path connects the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage.

10. (Currently amended) A test circuit for a logical integrated circuit having an input terminal, a functional output terminal, and a scan output terminal, said test circuit comprising:

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path ~~serially connecting said plurality of flip-flops,~~ to propagate a test pattern applied to the input terminal of one of said plurality of ~~serially connected~~ flip-flops, wherein:

the test pattern ~~measures~~ is used to measure an alternating current characteristic of the input terminal ~~or the functional output terminal~~ of said logical integrated circuit,

said scan path connects the scan input with the input terminal of the flip-flop located at the head of the nth stage,

~~from the output of the flip-flop located at the end of the nth stage, said scan path further connects the flip-flops in the second to the (n-1)th stages in series,~~

said scan path connects the output terminal of the flip-flop located at the end of the nth stage to the flip-flop at the head of the second stage,

said scan path then connects the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage, and

the scan path finally connects the output terminal of the flip-flop located at the end of

the first stage with the scan output terminal of said logical integrated circuit.

11. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

an input terminal,

a functional output terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~ and

means forming a scan path serially connecting said plurality of flip-flops, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of the input terminal ~~or the functional output terminal~~ of said logical integrated circuit by inspecting an output of the scan output terminal of said logical integrated circuit, said method comprising:

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the input terminal of said logical

integrated circuit by inspecting the output of the scan output terminal of said logical integrated circuit.

12. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a functional input terminal,

an output terminal,

a scan input terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops, ~~connected in series,~~ and

means forming a scan path serially connecting said plurality of flip-flops, to propagate a test pattern applied to the input terminal of one of said plurality of serially connected flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of ~~the functional input terminal or~~ the output terminal of said logical integrated circuit by inspecting an output of the output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the scan input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the output terminal of said logical integrated circuit by inspecting the output of the output terminal of said logical integrated circuit.

13. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a functional input terminal

a functional output terminal,

a scan input terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal, said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path ~~serially connecting said plurality of flip-flops,~~ to propagate a test pattern applied to the input terminal of one of said plurality of ~~serially connected~~ flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of the functional input terminal ~~or the functional output terminal~~ of said logical integrated circuit by inspecting an output of the scan output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

connecting the output terminal of the flip-flop located at the end of the nth stage with

the input terminal of the flip-flop located at the head of the second stage,

~~connecting the flip-flops in the second to the (n-1)th stages in series,~~

connecting the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage,

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a scan input signal to the scan input terminal of said logical integrated circuit,

inputting a predetermined data signal to the functional input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the functional input terminal of said logical integrated circuit by inspecting ~~an~~ the output of the scan output terminal of said logical integrated circuit.

14. (Currently amended) A method of testing a logical integrated circuit, the logical integrated circuit comprising:

a functional input terminal

a functional output terminal,

a scan input terminal,

a scan output terminal,

a plurality of flip-flops, each flip-flop having an input terminal and an output terminal,

said flip-flops being arranged in a matrix having n stages, each stage comprising m flip-flops connected in series, and

means forming a scan path ~~serially connecting said plurality of flip-flops,~~ to propagate a test pattern applied to the input terminal of one of said plurality of flip-flops, the test pattern ~~measuring~~ enabling measurement of an alternating current characteristic of ~~the functional input terminal or~~ the functional output terminal of said logical integrated circuit by inspecting an output of the output terminal of said logical integrated circuit, said method comprising:

connecting the scan input terminal of said logical integrated circuit with the input terminal of the flip-flop located at the head of the nth stage,

connecting the output terminal of the flip-flop located at the end of the nth stage with the input terminal of the flip-flop located at the head of the second stage,

~~connecting the flip-flops in the second to the (n-1)th stages in series,~~

connecting the output terminal of the flip-flop located at the end of the (n-1)th stage with the input terminal of the flip-flop located at the head of the first stage,

connecting the output terminal of the flip-flop located at the end of the first stage with the scan output terminal of said logical integrated circuit,

inputting a clock signal to a clock signal input terminal of each of said flip-flops,

inputting a predetermined data signal to the scan input terminal of said logical integrated circuit, and

measuring the alternating current characteristic of the functional output terminal of said logical integrated circuit by inspecting the output of the output terminal of said logical integrated circuit.